REMARKS/ARGUMENT

Claim 15 is amended. No new matter is added.

Claims 1, 2 and 4-8 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 3,980,959 to George ("George") in view of U.S. Patent No. 5,682,522 to Huang et al. ("Huang"). Claims 14 and 15 are rejected under 35 U.S.C. § 103 as being unpatentable over admitted prior art in view of Huang. Claim 3 is objected as being unpatentable over admitted prior art in view of George and further in view of U.S. Patent No. 5,982,781 to Przybyla et al. ("Przybyla") and U.S. Patent No. 5,570,306 to Soo ("Soo"). Claims 9 and 10 are rejected under 35 U.S.C. § 103 as being unpatentable over admitted prior art in view of George and further in view of Przybyla. Claims 11 and 12 are rejected as being unpatentable over admitted prior art in view George, Przybyla and Soo.

Reconsideration of the application in light of the remarks below is respectfully requested.

Independent claims 1, 2 and 15 recite a first path where video data is sent to a display through a frame buffer and a second, distinct or independent path which does not include the frame buffer and where video data is sent to a system memory. Similarly, independent claims 7 and 14 recite sending or forwarding video data to a display on a first path through a frame buffer and sending or forwarding video data to a system memory through a second path which does not include the frame buffer, where the first and second paths are independent or distinct.

The Office Action states that the second path recited in all the pending independent claims is not shown in the admitted prior art and points to the Huang reference for this feature. Specifically, the Office Action points to the paths G, F, E, and D shown in Fig. 3 of Huang as reading on the claimed second paths.

Paths A-G of Figure 3 are only logical paths used to describe possible data transfers in the system of Huang. The physical paths of the system are shown in Figure 2 and all include the single physical path (not labeled) connecting controller 15 and memory 5.

Huang discloses a system designed to solve the problem of memory resource use. See, e.g., column 1, lines 57-60. Huang solves this problem by combining frame buffer memory 51 and disk cache memory 52 into a single memory 5. By providing this solution, each of CPU 2, hard disk 4 and video display 3 must access this single memory 5 through a single memory controller 15 and the single physical path (not labeled) connecting controller 15 and memory 5.

Therefore, the Huang reference does not show two distinct or independent paths as is claimed.

It is asserted that independent claims 1, 2 and 7 are patentable over the art of record. Claims 3-6 and 8-12 are dependent upon claims 1, 2 and 7 respectively. These claims contain further limitations which, in combination with the limitations of independent claims 1, 2 and 7 are also neither disclosed nor suggested in the art of record. It is asserted that these claims are patentable as well. Reconsideration of the rejection of claims 1-14 under 35 U.S.C. § 103 is respectfully requested in light of the remarks above.

Respectfully submitted,

Dated: May 19, 2003

Steven S. Rubin
Registration No.: 43,063
DICKSTEIN SHAPIRO MORIN & OSHINSKY, LLP
1177 Avenue of the Americas
New York, New York 10036
Telephone: (212) 835-1400

SIW/SSR/mgs

APPENDIX A
Version With Markings To Show Changes Made
37 C.F.R. § 1.121(b)(1)(iii) AND (c)(1)(ii)

CLAIMS:

15. (Amended) A video data transfer system comprising:

a video processor which receives video data and processes the video data to produce processed video data; a display path coupled to the video processor, the display path including a frame buffer, the display path conveys the processed video data from the video processor to a display; and

a capturing path coupled to the video processor, the capturing path conveys the processed data from the video processor to a system memory, the capturing path not including the frame buffer, the capturing path being distinct from the display path.